TRANSISTOR-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD *COMPATIBLE CURRENT SINKING LOGIC* PRODUCT

MILITARY TEMPERATURE RANGE: −55°C to 125°C

GENERAL DESCRIPTION

The Fairchild Transistor-Transistor Micrologic® Integrated Circuit family (TTμL) combines a high fanout, high noise immunity, low power dissipation and good capacitive load driving capability with low propagation delay times.

The circuits are fabricated within a silicon monolithic substrate using standard Fairchild Planar† Epitaxial processes.

TTμL elements are available in two hermetically sealed ceramic packages; the Dual In-Line Package (DIP), designed for automated and low cost insertion techniques, and the 14 lead CERPAK® flat package.

Worst case curves of important device characteristics are offered to assist the designer in achieving maximum system reliability. For additional information refer to Application note No. 131.

FEATURES

- Single power supply requirement; 5 volts optimum, 4.5 to 5.5 volt range.
- Reliable operation over the full military temperature range of −55°C to 125° C.
- Guaranteed fanout of 10 TTμL loads over the full temperature and supply voltage range.
- Guaranteed minimum of 0.4 volt noise immunity at the temperature extremes.
- Typical "one" level noise immunity of 1.3 volts and "zero" level noise immunity of 0.8 volt.
- Typical power dissipation of 11 mW per gate at a 50% duty cycle.
- Typical logic gate propagation delays of 6 ns for 15 pF, 11 ns for 150 pF of capacitance.
- The unique output pull-up circuitry gives a higher output "one" level and can provide more output high current at low temperatures than conventional pull-ups.
- The input threshold of 1.5 volts and V_{CC} of 5 volts provides easy interfacing with the Fairchild DTμL family, and other DTL and TTL circuits.
- Nand gate pin configurations are compatible with DTμL.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

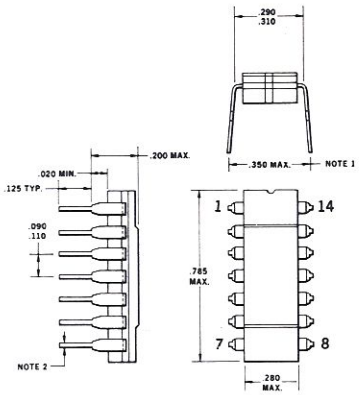
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} pin potential to ground	−.5 to +8 V
Input Voltage	−1.5 to +5.5 V
Gate Output Voltage, Inputs Low	−.5 to +V_{CC} value
Gate Current Into Output Terminal, Inputs High (except 9009)	50 mA
Gate Current Into Output Terminal, Inputs High 9009	100 mA
Flip-Flop Output Voltage when output is normally high	−.5 to +V_{CC} value
Flip-Flop Current Into Output Terminal when output is normally low	50 mA

ORDER INFORMATION

To order Transistor-Transistor Micrologic elements specify U31XXXX-51X for Flat package and U6AXXXX51X for Dual In-Line package where XXXX is the four-digit number denoting the specific element desired.

DUAL IN-LINE PACKAGE

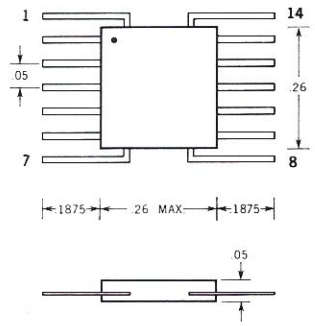
TO-116



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

FLAT PACKAGE

TOP VIEW



Flat-pack and Dual-in-line have same pin configurations.

† Planar is a patented Fairchild process.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

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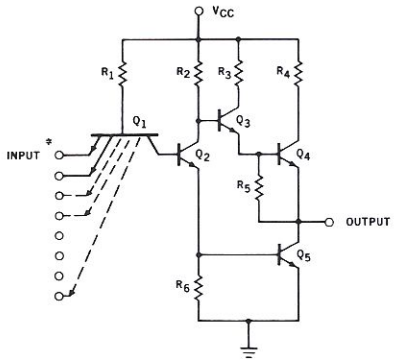
MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 291877, 3015048, 3025589, 3064167, 3108359, 3117260; OTHER PATENTS PENDING.

GATE ELEMENTS — 9002, 9003, 9004, 9007

All TTμL gates are positive logic NAND gates and negative logic NOR gates. A variety of gate combinations is available which provides the system designer the utmost in logic flexibility and reduces package requirements to a minimum.

BASIC GATE CIRCUIT

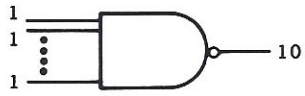


TYPICAL RESISTOR VALUES
$R_1 = R_5 = 4\ k\Omega$
$R_2 = 1.5\ k\Omega$
$R_3 = 150\ \Omega$
$R_4 = 80\ \Omega$
$R_6 = 1.25\ k\Omega$

*Number of inputs depends on the gate.

Figure 1

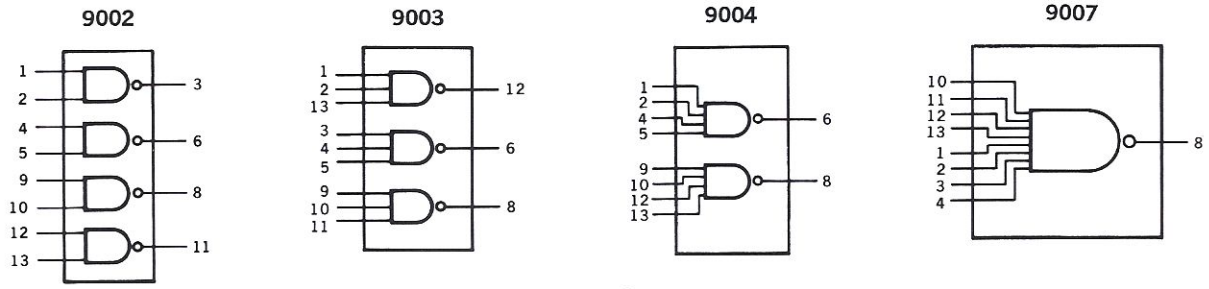
LOADING RULES



The outputs CANNOT be tied together for the "wired OR" function.

Figure 2

PIN CONFIGURATION



3a 3b 3c 3d

Figure 3

V_{CC} = PIN 14 GND = PIN 7

ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = 1.0\ mA$ V_{IL} = value indicated below on this table.
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 17.6\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 14.5\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs.
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs.
I_F	Input Load Current		−1.76		−1.10	−1.76		−1.76	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$, $V_R = 4.5\ V$ on other inputs
I_F	Input Load Current		−1.45		−0.97	−1.45		−1.45	mA	$V_{CC} = 4.5\ V$
I_R	Input Leakage Current				20	60		100	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$, Gnd. on other inputs
t_{pd+}	Turn Off Delay			4.0		12			ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ (see fig. 5b)
t_{pd-}	Turn On Delay			3.0		10			ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ (see fig. 5b)

GATE ELEMENTS — 9002, 9003, 9004, 9007 (continued)

WORST CASE LOGIC LEVELS VERSUS TEMPERATURE

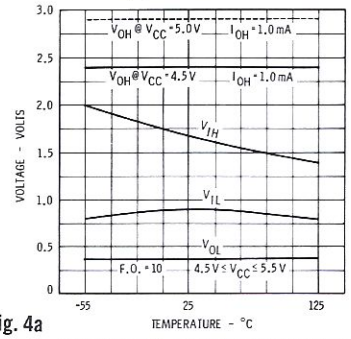


Fig. 4a

WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS TEMPERATURE

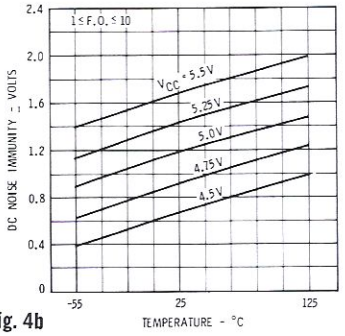


Fig. 4b

WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS TEMPERATURE

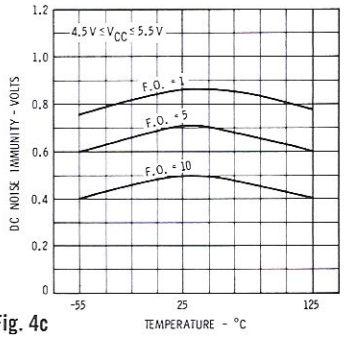


Fig. 4c

WORST CASE POWER DISSIPATION VERSUS SUPPLY VOLTAGE (PER GATE)

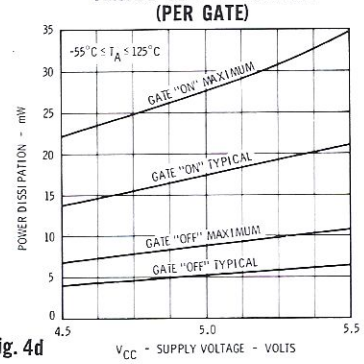


Fig. 4d

WORST CASE POWER DISSIPATION VERSUS FREQUENCY (PER GATE)

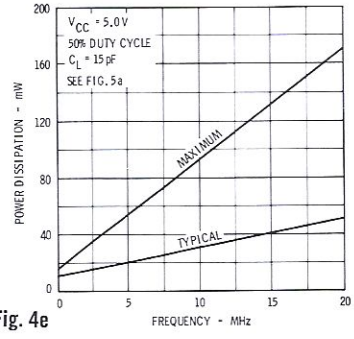


Fig. 4e

WORST CASE TURN OFF DELAY VERSUS TEMPERATURE

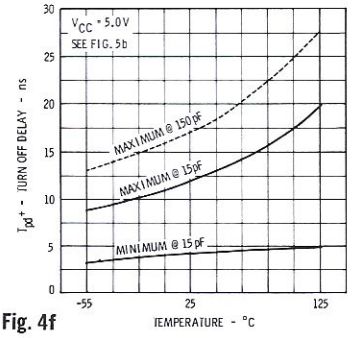


Fig. 4f

WORST CASE TURN ON DELAY VERSUS TEMPERATURE

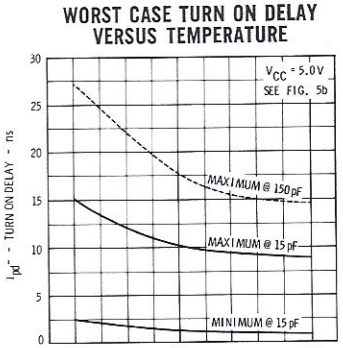
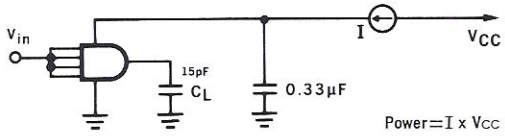


Fig. 4g

FIGURE 4

AC POWER TEST CIRCUIT



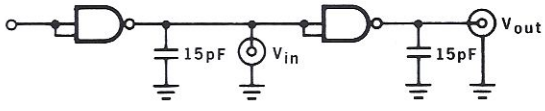
V_{in}
50% Duty Cycle
Amp ≃ 4 V
$t_r = t_f \leq 10$ ns

FIGURE 5a

NOTE: Capacitance includes probe and jig capacity. All inputs are to be tied together.

tpd TEST CIRCUIT

f ≃ 1 MHz
Amp ≃ 4 V
Width ≃ 200 ns
$t_r = t_f \leq 10$ ns



SWITCHING WAVEFORM

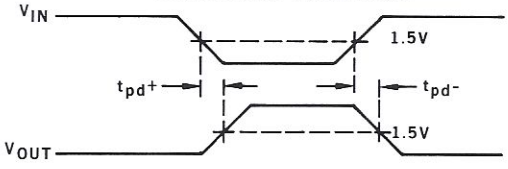


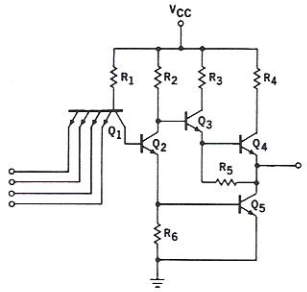
FIGURE 5b

NOTE: Capacitance includes probe and jig capacity. All inputs are to be tied together.

POWER GATE ELEMENT — 9009

The TTμL 9009 element is a NAND power gate capable of driving and sinking large currents for high fan-out applications.

For noise immunity and operating level curves, refer to the gate section.



TYPICAL RESISTOR VALUES

$R_1 = 2.2k\Omega$ $R_4 = 50\Omega$

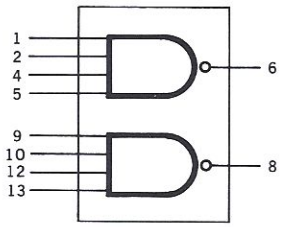
$R_2 = 450\Omega$ $R_5 = 4k\Omega$

$R_3 = 150\Omega$ $R_6 = 400\Omega$

LOADING RULES:

The outputs CANNOT be tied together for the "wired OR" function.

PIN CONFIGURATION



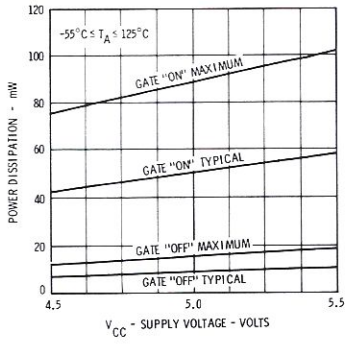
V_{CC} = PIN 14 GND = PIN 7

ELECTRICAL CHARACTERISTICS

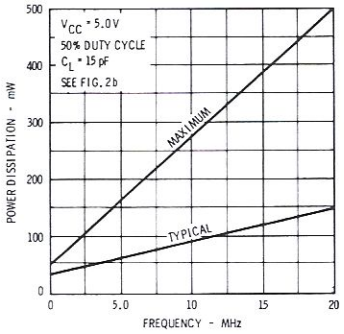
SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS & COMMENTS	
		−55°C		25°C			125°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.			
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4	Volts	V_{CC} = 4.5 V, I_{OH} = 3.0 mA V_{IL} = value indicated below on this table.	
V_{OL}	Output Low Voltage		0.4		0.2	0.4	0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 52.8 mA V_{CC} = 4.5 V, I_{OL} = 42.9 mA	
V_{IH}	Input High Voltage	2.0		1.7			1.4	Volts	Guaranteed input high threshold for all inputs.	
V_{IL}	Input Low Voltage		0.8			0.9	0.8	Volts	Guaranteed input low threshold for all inputs.	
I_F	Input Load Current		− 3.52		− 1.95	− 3.52	− 3.52	mA	V_{CC} = 5.5 V	V_F = 0.4 V, V_R = 4.5 V on other inputs
I_F	Input Load Current		− 2.9		− 1.6	− 2.9	− 2.9	mA	V_{CC} = 4.5 V	
I_R	Input Leakage Current				35	120	200	μA	V_{CC} = 5.5 V, V_R = 4.5 V, Gnd. on other inputs.	
t_{pd+}	Turn Off Delay			4.0		17		ns	V_{CC} = 5.0 V, C_L = 15 pF (see fig. 2a)	
t_{pd-}	Turn On Delay			3.0		10		ns	V_{CC} = 5.0 V, C_L = 15 pF (see fig. 2a)	

POWER GATE ELEMENT — 9009 (continued)

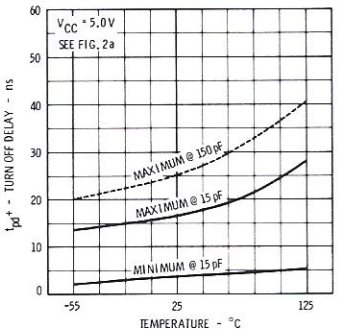
WORST CASE POWER DISSIPATION VERSUS COLLECTOR SUPPLY VOLTAGE (PER GATE)



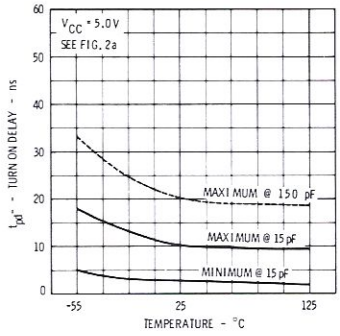
WORST CASE POWER DISSIPATION VERSUS FREQUENCY (PER GATE)



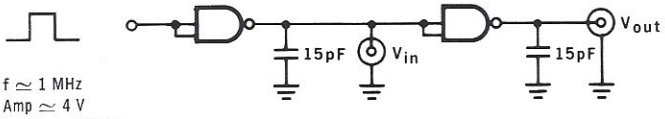
WORST CASE TURNOFF DELAY VERSUS TEMPERATURE



WORST CASE TURN ON DELAY VERSUS TEMPERATURE

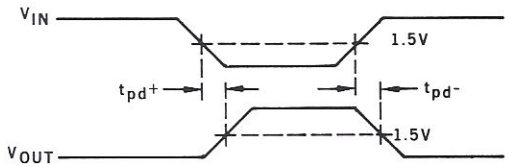


tpd TEST CIRCUIT



f ≃ 1 MHz
Amp ≃ 4 V
Width ≃ 200 ns
$t_r = t_f \leq 10$ ns

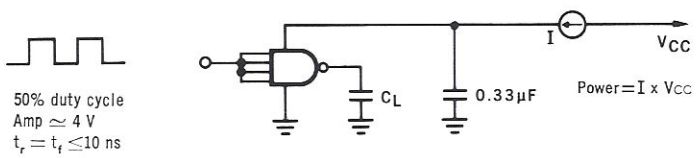
SWITCHING WAVEFORM



NOTE: Capacitance includes probe and jig capacity.
All inputs are to be tied together.

FIGURE 2a

AC POWER TEST CIRCUIT



50% duty cycle
Amp ≃ 4 V
$t_r = t_f \leq 10$ ns

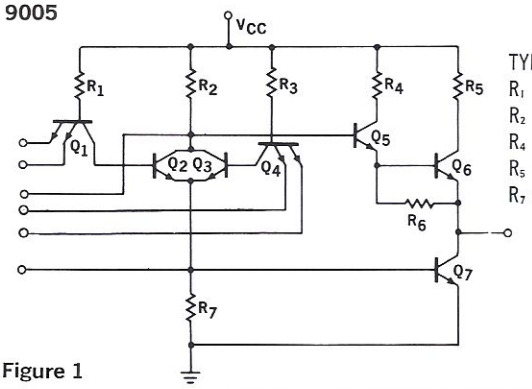
NOTE: Capacitance includes probe and jig capacity.
All inputs are to be tied together.

FIGURE 2b

EXPANDABLE GATES — 9005, 9006, 9008

The TTμL 9005 and 9008 are AND-NOR gates which may be NOR expanded with the use of the 9006 element. For noise immunity and operating level curves, refer to the gate section.

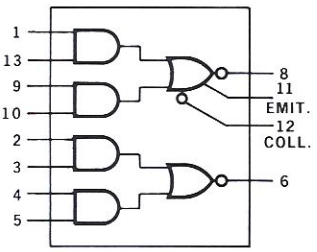
9005



TYPICAL RESISTOR VALUES
$R_1 = R_3 = R_6 = 4\ k\Omega$
$R_2 = 1.5\ k\Omega$
$R_4 = 150\ \Omega$
$R_5 = 80\ \Omega$
$R_7 = 1.25\ k\Omega$

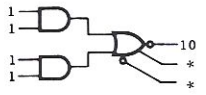
Figure 1

PIN CONFIGURATION



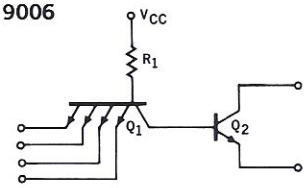
V_{CC} = PIN 14 GND = PIN 7

LOADING RULES:



*Four Expanders (9006) may be tied to these terminals.

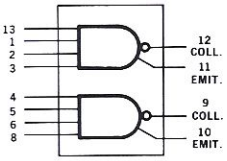
9006



TYPICAL RESISTOR VALUE
$R_1 = 4\ k\Omega$

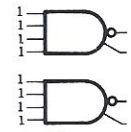
Figure 2

PIN CONFIGURATION

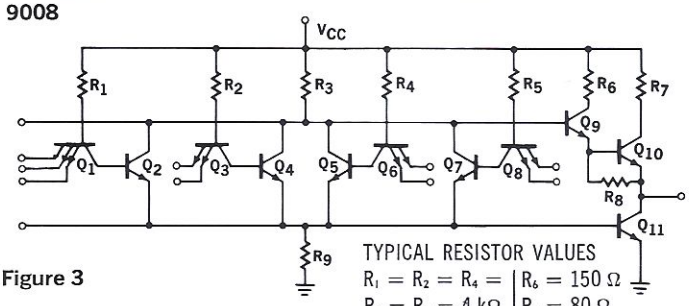


V_{CC} = PIN 14 GND = PIN 7

LOADING RULES:



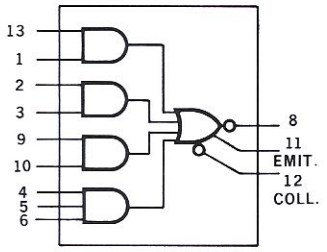
9008



TYPICAL RESISTOR VALUES
$R_1 = R_2 = R_4 = R_5 = R_8 = 4\ k\Omega$
$R_3 = 1.5\ k\Omega$
$R_6 = 150\ \Omega$
$R_7 = 80\ \Omega$
$R_9 = 1.25\ k\Omega$

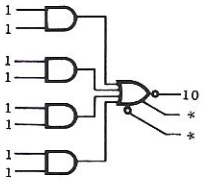
Figure 3

PIN CONFIGURATION



V_{CC} = PIN 14 GND = PIN 7

LOADING RULES:



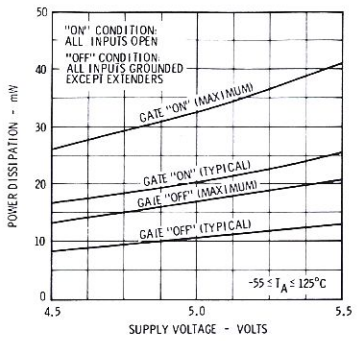
*Four Expanders (9006) may be tied to these terminals.

ELECTRICAL CHARACTERISTICS

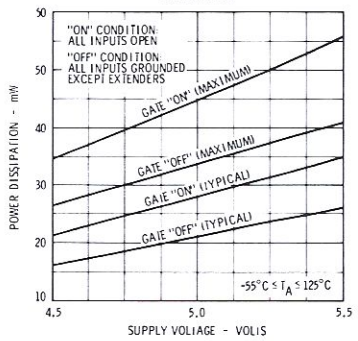
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = 1.0\ mA$ V_{IL} = value indicated below on this table
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 17.6\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 14.5\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs.
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs.
I_F	Input Load Current		−1.76		−1.10	−1.76		−1.76	mA	$V_{CC} = 5.5\ V$; $V_F = 0.4\ V$, $V_R = 4.5\ V$ on other inputs
I_F	Input Load Current		−1.45		−0.97	−1.45		−1.45	mA	$V_{CC} = 4.5\ V$; $V_F = 0.4\ V$, $V_R = 4.5\ V$ on other inputs
I_R	Input Leakage Current				20	60		100	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$, Gnd. on other inputs
t_{pd+}	Defined in Test Circuit			4		12			ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ Applies to 9005 nonexpandable Gate only
t_{pd-}	Defined in Test Circuit			3		12			ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ Applies to 9005 nonexpandable Gate only
t_{pd+}	Defined in Test Circuit			4		15			ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$, $C_N = 5.0\ pF$ Applies to 9008 and 9005 Expandable Gate
t_{pd-}	Defined in Test Circuit			3		10			ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$, $C_N = 5.0\ pF$ Applies to 9008 and 9005 Expandable Gate
Δt_{pd+}	See Comment			0		4			ns	9006 only
Δt_{pd-}	See Comment			0		4			ns	The 9006 shall be tested by measuring its propagation time through the 9005. The t_{pd} reading shall not exceed the 9005 reading by the specified amount.

EXPANDABLE GATES — 9005, 9006, 9008 (continued)

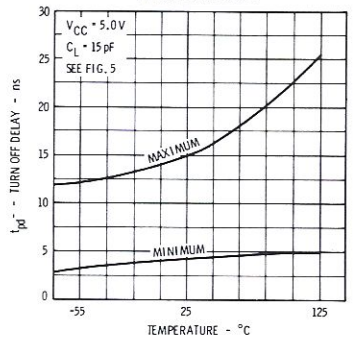
WORST CASE POWER DISSIPATION OF 9005 VERSUS SUPPLY VOLTAGE (PER GATE)



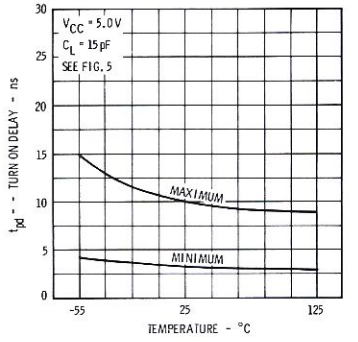
WORST CASE POWER DISSIPATION OF 9008 VERSUS SUPPLY VOLTAGE



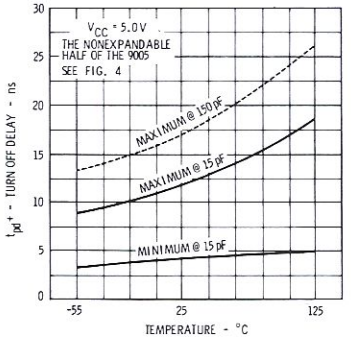
WORST CASE TURN OFF DELAY OF EXPANDABLE GATE VERSUS TEMPERATURE



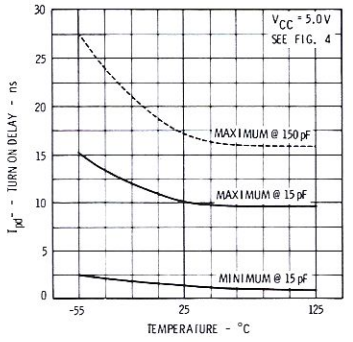
WORST CASE TURN ON DELAY OF EXPANDABLE GATE VERSUS TEMPERATURE



WORST CASE TURN OFF DELAY OF NONEXPANDABLE GATE VERSUS TEMPERATURE

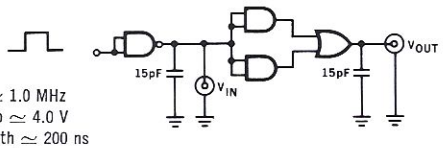


WORST CASE TURN ON DELAY OF NONEXPANDABLE GATE VERSUS TEMPERATURE



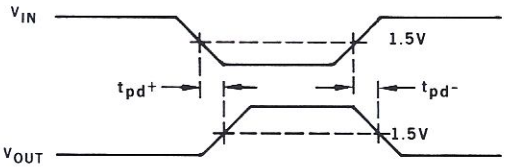
tpd TEST CIRCUIT

9005 NONEXPANDABLE GATE ONLY



f ≃ 1.0 MHz
Amp ≃ 4.0 V
Width ≃ 200 ns
$t_r = t_f \leq 10$ ns

SWITCHING WAVEFORM



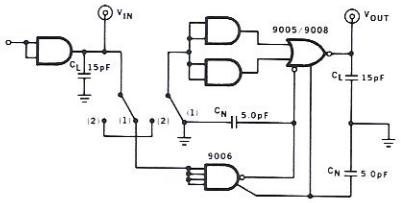
NOTE: Capacitance includes probe and jig capacity.
All inputs are to be tied together.

Figure 4

tpd TEST CIRCUIT

9005/9008 EXPANDABLE GATE AND 9006 EXPANDER

f ≃ 1.0 MHz
Amp ≃ 4.0 V
Width ≃ 200 ns
$t_r = t_f \leq 10$ ns



NOTE: Position (2) is used to test 9005/9008.
Position (1) is used to test 9006.
Capacitance includes probe and jig capacity.

Figure 5

J-K FLIP-FLOPS — 9000, 9001

GENERAL DESCRIPTION — The TTμL family includes the 9000 and 9001 flip-flops to satisfy the storage element needs of a logic system. Each is a master-slave JK flip-flop with the same multi-emitter inputs and low impedance active pull-up outputs common to the gate elements.

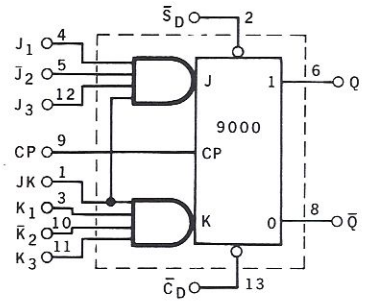
The internal JK connections assure the user of non-ambiguous operation for all input states. The master-slave design with buffered clock input offers high noise immunity, low clock loading and eliminates the need for careful control of clock pulse rise or fall times. Data is accepted by the master when the clock is in the low logic state. Transfer from master to slave occurs when the clock goes from the low to the high logic level. When the clock is in the high logic level both J and K inputs are inhibited. For this reason it is desirable to maintain the clock pulse in the high level most of the duty cycle. Direct set and reset inputs provide true asynchronous control of both master and slave flip-flops independent of logic and clock input levels.

A common J-K input is provided which is useful in the physical layout of most logic configurations.

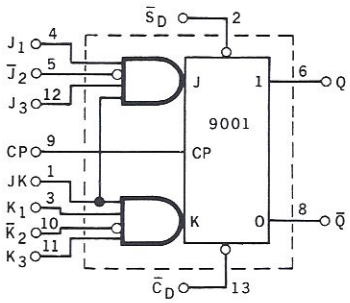
The two circuits are identical with a few exceptions. The 9000 has capacitors at the outputs of the J and K data input gates in the master flip-flop. The capacitors serve to lengthen the time requirements between J or K data and the low-to-high clock transition. This feature makes the 9000 particularly attractive for applications where clock skew is an important consideration.

The 9001 provides one $\overline{J}$ and one $\overline{K}$ input for additional logic flexibility. It has no master flip-flop capacitors to extend the set-up time and therefore has a higher toggling rate.

The important characteristics of the two flip-flops are illustrated in the following curves and specifications. Noise immunity and operating level curves shown in the gate section of the data sheet are applicable to the flip-flops as well.



VCC = PIN 14
GND = PIN 7



V_{CC} = PIN 14
GND = PIN 7

LOADING RULES

FLIP-FLOP INPUTS	LOADING*
CP, J_1, J_2, J_3, K_1, K_2, K_3, $\overline{J}_2$, $\overline{K}_2$,	1
JK	2
$\overline{S}_D$, $\overline{C}_D$	2.7

OUTPUTS	FAN-OUT
Q, $\overline{Q}$	10

*1 load = 1 TTμL Gate Input Load

TRUTH TABLES

SYNCHRONOUS ENTRY
J-K MODE OPERATION

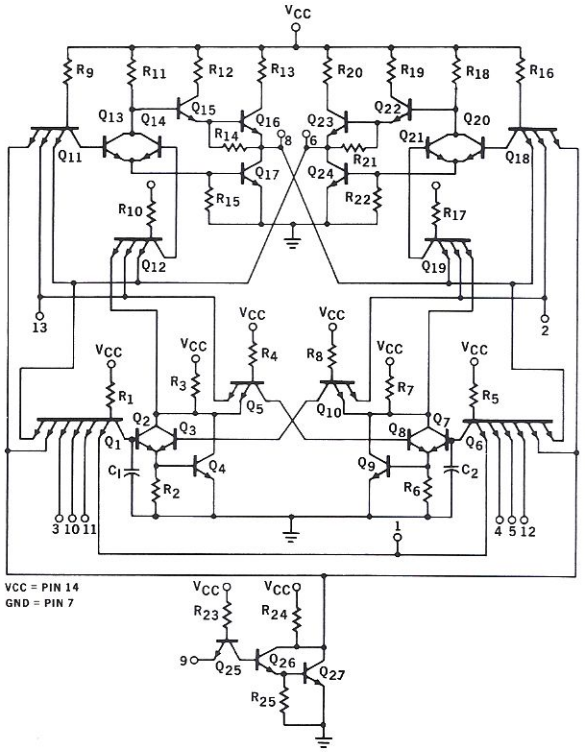
INPUTS @ t_n			OUTPUTS @ t_{n+1}	
JK	(5) $J_1 \cdot J_2 \cdot J_3$	(5) $K_1 \cdot K_2 \cdot K_3$	Q	$\overline{Q}$
1	4 5 12	3 10 11	6	8
L	X	X	No Change (4)	
H	L	L	No Change (4)	
H	L	H	L	H
H	H	L	H	L
H	H	H	Toggles	

ASYNCHRONOUS ENTRY
Independent of Clock and Synchronous Input

INPUTS		OUTPUTS	
S_D	C_D	Q	$\overline{Q}$
2	13	6	8
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

NOTES:
(1.) H = Most positive logic level.
(2.) L = Most negative voltage level.
(3.) X = Could be high or low.
(4.) For no change of outputs, the J and K inputs or the common JK input must remain low from the time the clock goes low to the time the clock goes high again.
(5.) The 9001 has inverted J_2 (Pin 5) and K_2 (Pin 10) inputs. When not in use, they must be grounded.

9000 SCHEMATIC DIAGRAM

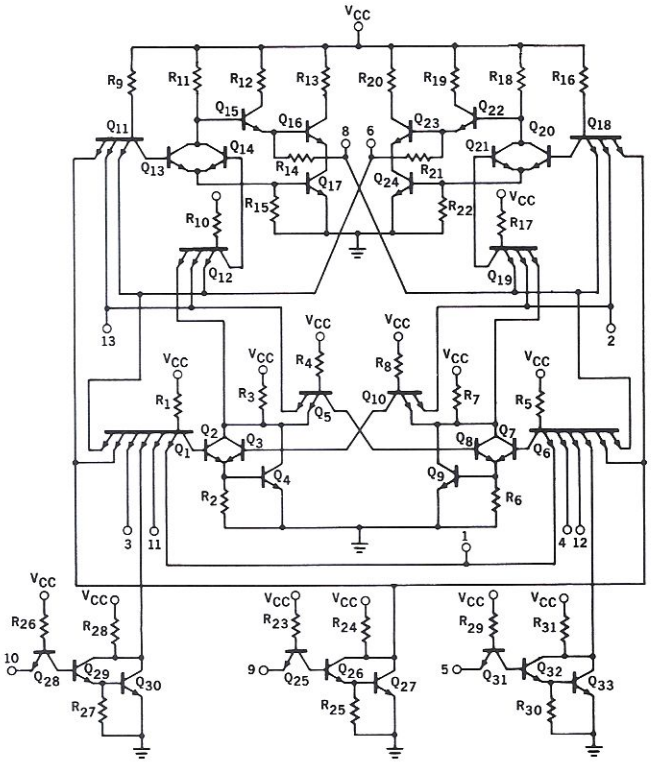


TYPICAL COMPONENT VALUES

$R_1, R_4, R_5, R_8, R_{10}$,
$R_{14}, R_{17}, R_{21}, R_{22}, R_{23}, R_{24} = 4\ k\Omega$
$R_2, R_3, R_6, R_7 = 2\ k\Omega$
$R_9, R_{16} = 6\ k\Omega$
$R_{11}, R_{18} = 1.5\ k\Omega$
$R_{12}, R_{19} = 150\ \Omega$
$R_{13}, R_{20} = 80\ \Omega$
$R_{15}, R_{22}, R_{25} = 1.25\ k\Omega$
$C_1, C_2 = 10\ pF$

Figure 6

9001 SCHEMATIC DIAGRAM



TYPICAL COMPONENT VALUES

$R_1, R_4, R_5, R_8, R_{10}, R_{14}, R_{17}, R_{21}$,
$R_{22}, R_{23}, R_{24}, R_{26}, R_{29} = 4\ k\Omega$
$R_2, R_3, R_6, R_7 = 2\ k\Omega$
$R_9, R_{16}, R_{28}, R_{31} = 6\ k\Omega$
$R_{11}, R_{18} = 1.5\ k\Omega$
$R_{12}, R_{19} = 150\ \Omega$
$R_{13}, R_{20} = 80\ \Omega$
$R_{15}, R_{22}, R_{25}, R_{27}, R_{30} = 1.25\ k\Omega$

Figure 7

9000 AND 9001 FUNCTIONAL LOGIC DIAGRAM

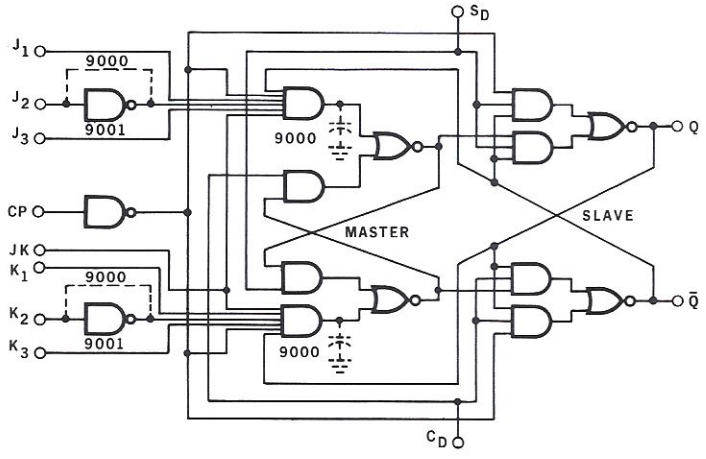


Figure 8

J-K FLIP-FLOPS — 9000, 9001 (continued)

ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = 1.0 mA, V_{IL} on asynchronous input	
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 14.5 mA V_{CC} = 5.5 V, I_{OL} = 17.7 mA	
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs	
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs	
I_R $2\ I_R$ I_{RS}	Input Leakage Current J, K, J, K & Clock Inputs J-K Input Asynchronous Inputs				20 40 55	60 120 162		100 200 270	μA	V_{CC} = 5.5 V, V_R = 4.5 V, Gnd. on other inputs	
I_F $2\ I_F$ I_{FSI}	Input Load Current J, K, J, K & Clock Inputs J-K Input Asynchronous Inputs		−1.76 −3.52 −4.75		−1.1 −2.2 −3.0	−1.76 −3.52 −4.75		−1.76 −3.52 −4.75	mA	V_{CC} = 5.5 V V_{CC} = 5.5 V V_{CC} = 5.5 V	V_F = 0.4 V V_R = 4.5 V on other inputs
I_F $2\ I_F$ I_{FSI}	Input Load Current J, K, J, K & Clock Inputs J-K Input Asynchronous Inputs		−1.45 − 2.9 − 3.92		−0.91 −1.82 −2.48	−1.45 − 2.9 −3.92		−1.45 −2.9 −3.92	mA	V_{CC} = 4.5 V V_{CC} = 4.5 V V_{CC} = 4.5 V	
t_{pd+}				—	12	20			ns	9000 or 9001	V_{CC} = 5.0 V C_L = 15 pF See test circuits and curves.
t_{pd-}				—	18	30			ns	9000 or 9001	
$t_{release}$	See Fig. 8				5	1			ns	9001 only	
t_{set-up}	See Fig. 8			10	6				ns	9001 only	
	Negative Clock pulse width			15	10				ns	9001 only Toggle condition	

WORST CASE POWER DISSIPATION VERSUS CLOCK INPUT FREQUENCY

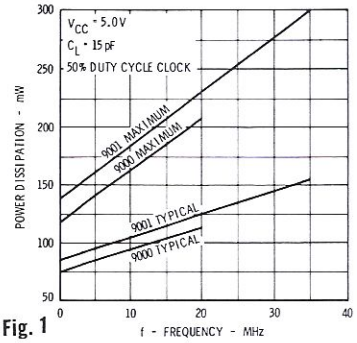


Fig. 1

9000 & 9001 WORST CASE MAX. & MIN. t_{pd+} & t_{pd-} PROPAGATION DELAYS — CP TO OUTPUTS

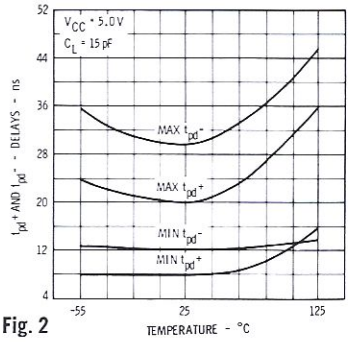


Fig. 2

9000 & 9001 WORST CASE MAX. & MIN. t_{pd+} & t_{pd-} PROPAGATION DELAYS — ASYNCHRONOUS INPUTS TO OUTPUTS

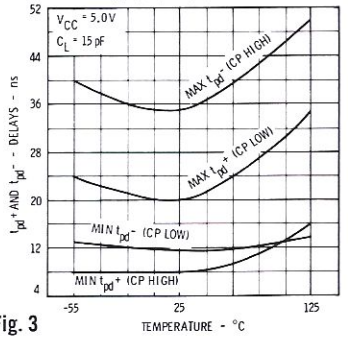


Fig. 3

INCREASE IN ASYNCHRONOUS OR CLOCK INPUT t_{pd+} AND t_{pd-} DUE TO OUTPUT CAPACITANCE

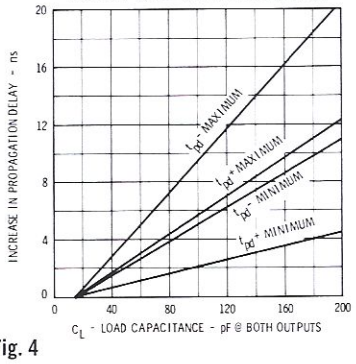


Fig. 4

9001 WORST CASE SET-UP/RELEASE TIME & NEG. CLOCK PULSE WIDTH

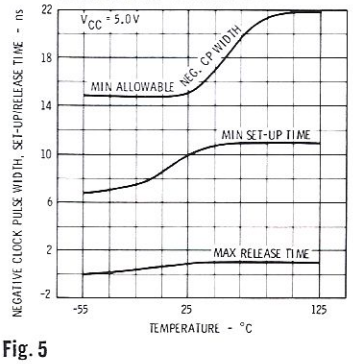

V_{CC} = 5.0V
MIN ALLOWABLE NEG. CP WIDTH
MIN SET-UP TIME
MAX RELEASE TIME
NEGATIVE CLOCK PULSE WIDTH, SET-UP/RELEASE TIME - ns
TEMPERATURE - °C

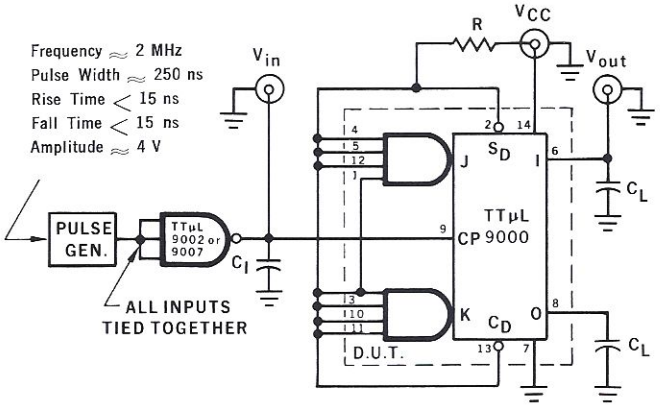
Fig. 5

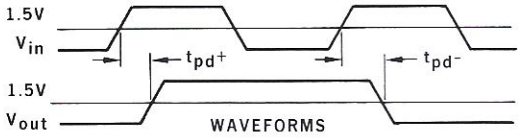
J-K FLIP-FLOPS — 9000, 9001 (continued)

SWITCHING TIME TEST CIRCUITS

9000

t_{pd+} and t_{pd-}



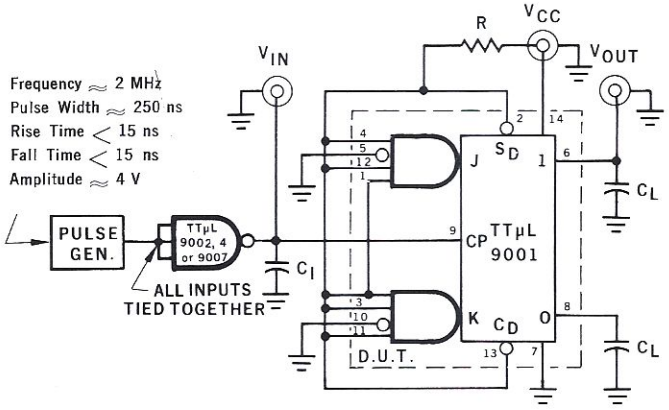


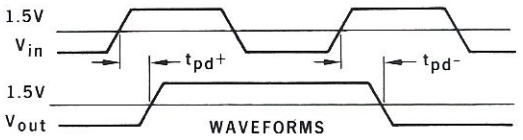
R = 2 K ±5% ½ W
C_I = 15 pF ± 5%
C_L = 15 pF ±5%

Figure 9

9001

t_{pd+} and t_{pd-}





R = 2 K ±5% ½ W
C_I = 15 pF ± 5%
C_L = 15 pF ±5%

Figure 10

SWITCHING NOTES

(1) The load capacitance indicated in test circuits includes the capacitance of probe and jig.

(2) All curves represent worst case composites of the behavior of limit devices. A typical device will not necessarily follow the temperature trend indicated by the curve, but should always be better than the worst case curve at any temperature in the range.

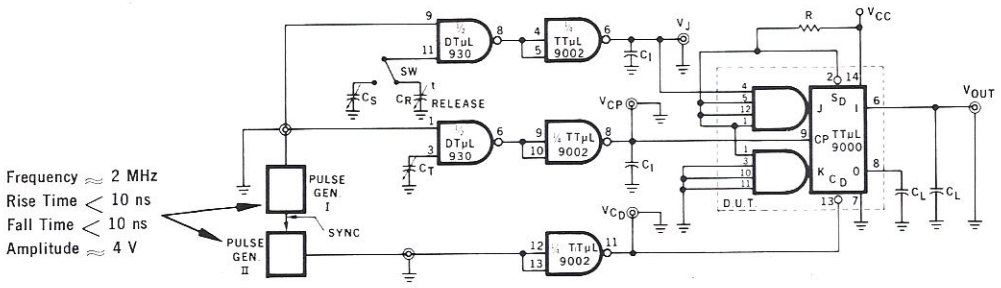
(3) Sensitivity of all switching parameters to supply voltage change (within range of 5 V ± 10%) and D.C. loading is very small.

(4) Figure 4 should be used with Figs. 2 and 3 to determine worst case delays with capacitive loading greater than 15 pF.

(5) Allowable clock skew $\leq t_{pd+}$ (min.) $+ t_{release}$ (max.)

J-K FLIP-FLOPS — 9000, 9001 (continued)

9000 t_{set-up} and $t_{release}$ TEST CIRCUIT



INITIAL ADJUSTMENT

1. With switch in t release position adjust pulse generators, C_T & C_R for proper V_{CP}, V_J & V_D waveforms and t release limit value.
2. With switch in t set-up position adjust C_S for t set-up limit value

t set-up is defined as the minimum time required for a ONE to be present at the logic input prior to the clock transition from low to high in order for the flip flop to respond.

t release is defined as the maximum time allowed for a ONE to be present at the logic inputs prior to the clock transition from low to high in order for the flip flop **not** to respond.

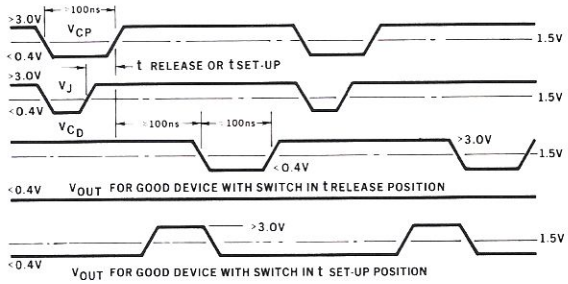
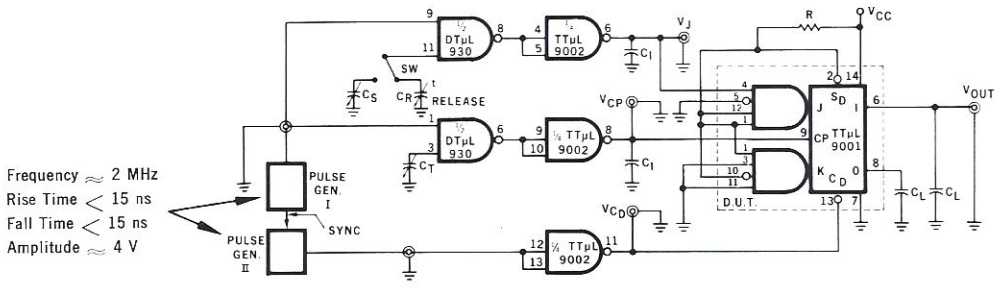


Figure 11

9001 t_{set-up} and $t_{release}$ TEST CIRCUIT



INITIAL ADJUSTMENT

1. With switch in t release position adjust pulse generators, C_T & C_R for proper V_{CP}, V_J & V_D waveforms and t release limit value.
2. With switch in t set-up position adjust C_S for t set-up limit value

t set-up is defined as the minimum time required for a ONE to be present at the logic input prior to the clock transition from low to high in order for the flip flop to respond.

t release is defined as the maximum time allowed for a ONE to be present at the logic inputs prior to the clock transition from low to high in order for the flip flop **not** to respond.

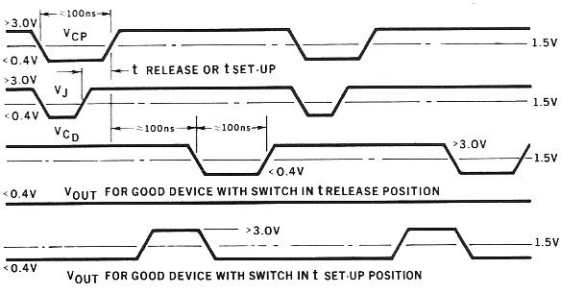


Figure 12

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